Table of Contents

Single-Channel Single-Output Touch IC

Document No.: PT-DS26007

1. Product Overview

PT2041B is a single-channel touch detection IC. An internal voltage regulator supplies stable bias voltage for touch sensing circuitry. Equipped with mature high-efficiency touch detection algorithm, the device delivers stable touch performance. Designed to replace conventional mechanical keys, it features wide supply voltage range and ultra-low power consumption, suitable for various consumer electronics applications.

2. Key Features

- Operating supply voltage: 2.0 ~ 5.5V
- Superior anti-interference performance: built-in regulator, power-on reset, brown-out reset and adaptive environmental tracking algorithm
- Typical standby current: 1.5μA @ VDD=3V, no load
- Typical response delay in low-power mode: 100ms @ VDD=3V
- Touch sensitivity adjustable via external 1~50pF capacitor
- Configurable output via TOG pin: synchronous output or toggle latch output
- QC CMOS output polarity configurable via AHLB: active-high or active-low
- Maximum continuous output holding time: 16 seconds
- 0.4s initialization period after power-up; touch input is invalid and all functions disabled during initialization
- Available packages: SOT23-6、DFN2*2-6L、DFN1*1-4L
- Not recommended for resistance-capacitance step-down power supply or systems with excessive power ripple; only for battery-powered products with low supply ripple.
- Select PT2022T6 for applications requiring higher noise immunity.

3. System Block Diagram

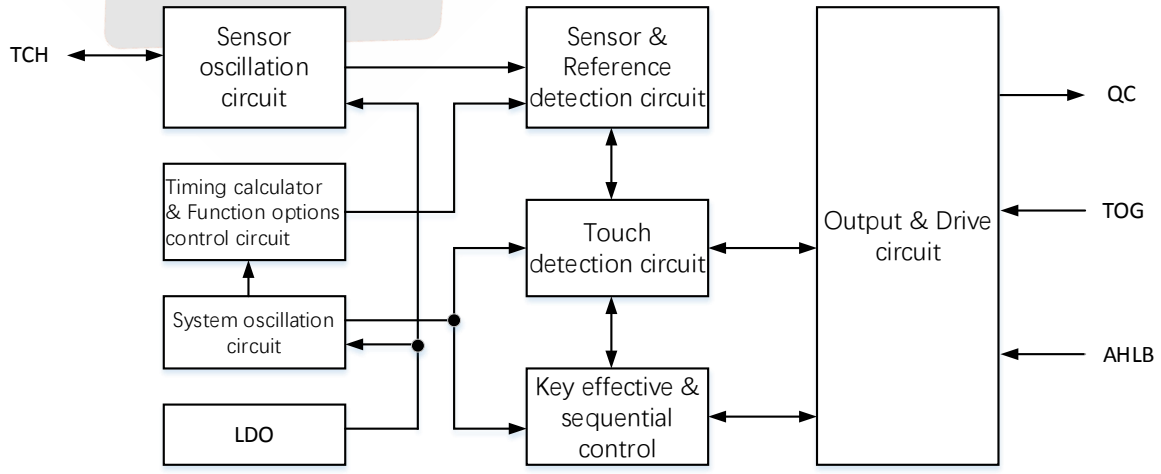


Figure1 System Block Diagram

4. Package and Pin Description

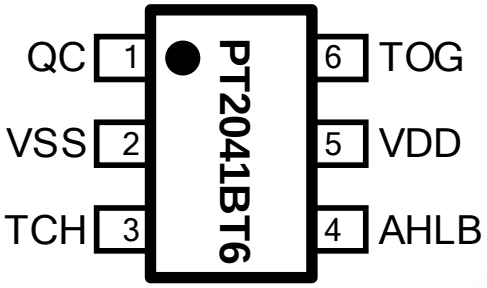


Figure2 SOT23-6 Pinout Diagram

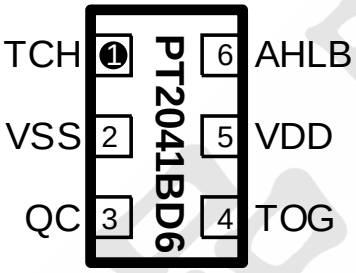


Figure3 DFN2x2-6L Pinout Diagram

Note：DFN pin assignment is mirrored versus SOT23-6.

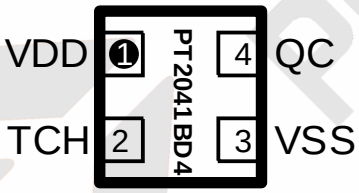


Figure4 DFN1x1-4L Pinout Diagram

Note：Fixed as synchronous output mode,active high.

Table1 Pin Definition

Pin Name	I/O	Description
QC	O	CMOS output pin
VSS	P	Ground reference
TCH	I	Touch sensing input
AHLB	I-PL	Select active-high or active-low output level AHLB=Floating/VSS（default）：Active-High； AHLB=VDD：Active-Low
VDD	P	Power supply input
TOG	I-PL	Select synchronous or toggle latch output TOG=Floating/VSS（default）：Synchronous output； TOG=VDD：Toggle latch output

Pin Type Definition：

I： CMOS Input

O： CMOS Output

I/O： CMOS Input/Output

P： Power/Ground

I-PH： CMOS input with internal pull-up

I-PL： CMOS input with internal pull-down

5. Function Description

5.1 Output Mode and Option Pins

- AHLB and TOG are latch-type option pins; default logic level = 0 after power-on. Level changes to 1 if tied to VDD before power-up with no DC leakage current.
- TOG：selects synchronous or toggle latch output.
- AHLB：selects active-high or active-low for QC output.

Option Features of QC Pin (CMOS Output)：

TOG	AHLB	QC Output Configuration
0	0	Synchronous,Active-High
0	1	Synchronous,Active-Low
1	0	Toggle latch, initial state = 0 at power-up
1	1	Toggle latch, initial state = 1 at power-up

5.2 Maximum Output Duration

- Persistent effective touch caused by panel coverage or abrupt ambient variation triggers auto-reset after continuous 16s valid output; IC restores to initial power-up state and QC turns inactive.

5.3 Low-Power Mode

- Enter low-power mode 1s after power-up for production test purpose
- Return to low-power mode after 8s idle without any touch event post key wake-up

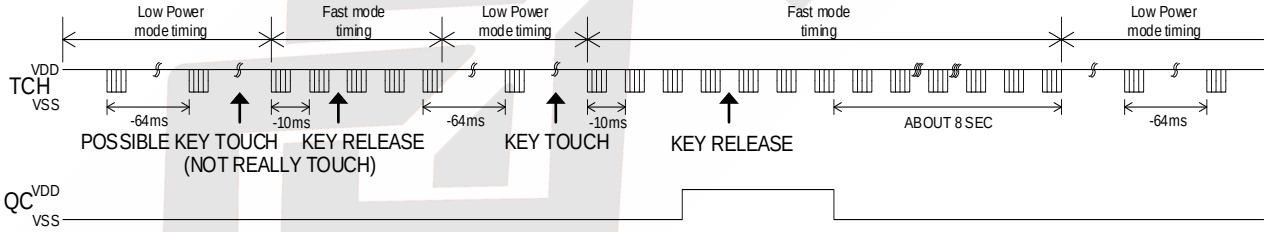


Figure4 Timing Diagram

5.4 Sensitivity Adjustment

Equivalent parasitic capacitance on TCH dominates touch sensitivity; tune parameters per actual PCB layout：

1) Touch pad dimension：
   Larger pad improves sensitivity, smaller pad reduces sensitivity within valid specification range.
2) Cover dielectric thickness：
   Thinner overlay raises sensitivity; thicker overlay degrades sensitivity.
3) External Cs capacitor
   Maximum sensitivity with no Cs connected to TCH-GND; higher Cs value reduces sensitivity. Cs range: 1pF ≤ Cs ≤50pF.

6. Application Circuit

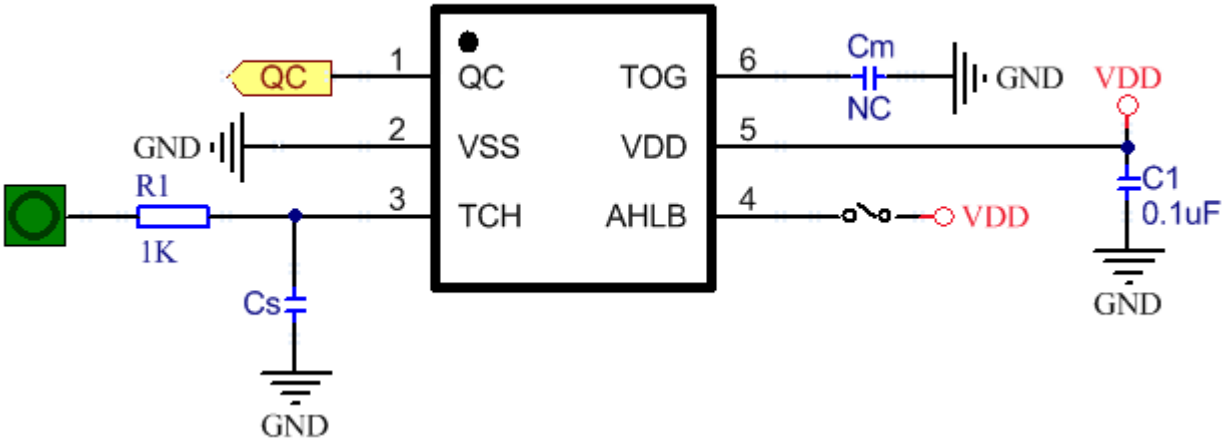


Figure5 Typical Application Schematic

Note：

1) Minimize routing length between touch pad and TCH; avoid parallel/cross routing with other traces.
2) Stable supply voltage required; fast supply fluctuation causes false trigger or abnormal sensitivity.
3) Covering dielectric shall contain no metallic or conductive materials including surface coating.
4) Place 104 or larger decoupling capacitor directly across VDD & VSS with shortest copper route to IC pins.
5) Cs (1~50pF) adjusts sensitivity; smaller Cs gives higher sensitivity, value defined per actual PCB.
6) Select low temperature drift capacitors such as NPO/X7R for Cs; NPO is preferred to minimize temperature-induced sensitivity shift.

7. Electrical Characteristics

7.1 Absolute Maximum Ratings

Table2 Absolute Maximum Ratings

Parameter	Symbol	Condition	Range	Unit
Supply Voltage	V_{DD}	-	-0 to +5.5	V
Input Voltage	V_I	All I/O Pins	-0.3 to V_{DD}+0.3	V
Operating Temp	T_A	-	-40~ +85	℃
Storage Temp	T_{STG}	-	-50~ +125	℃

7.2 DC Characteristics

Table3 VDD=2.0~5.5V, TA=25℃ unless specified otherwise

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	V_{DD}		2.0	3	5.5	V
Input High Level	V_{IH}	V_{DD}=5V,AHLB	0.7*VDD			V
		V_{DD}=5V,TOG				
Input Low Level	V_{IL}	V_{DD}=5V,AHLB			0.3*VDD	V
		V_{DD}=5V,TOG				
Source Current	I_{OH}	V_{DD}=3V, VOH=2.7V		4		mA
Sink Current	I_{OL}	V_{DD}=3V, VOL=0.3V		20		mA
Pull-down Resistor	R_{PL}	V_{DD}=3V（TOG、AHLB）	24	30	36	Kohm
Response Time	T_R	V_{DD}=3V,Fast Mode		40		ms
		V_{DD}=3V,Low-Power Mode		100		
Standby Current	I_{SB}	V_{DD}=3V,Low-Power, No Load		1.5	2.0	uA
		V_{DD}=3V,Fast Mode, No Load		8	10	

8. Package Specification

8.1 SOT23-6 Package

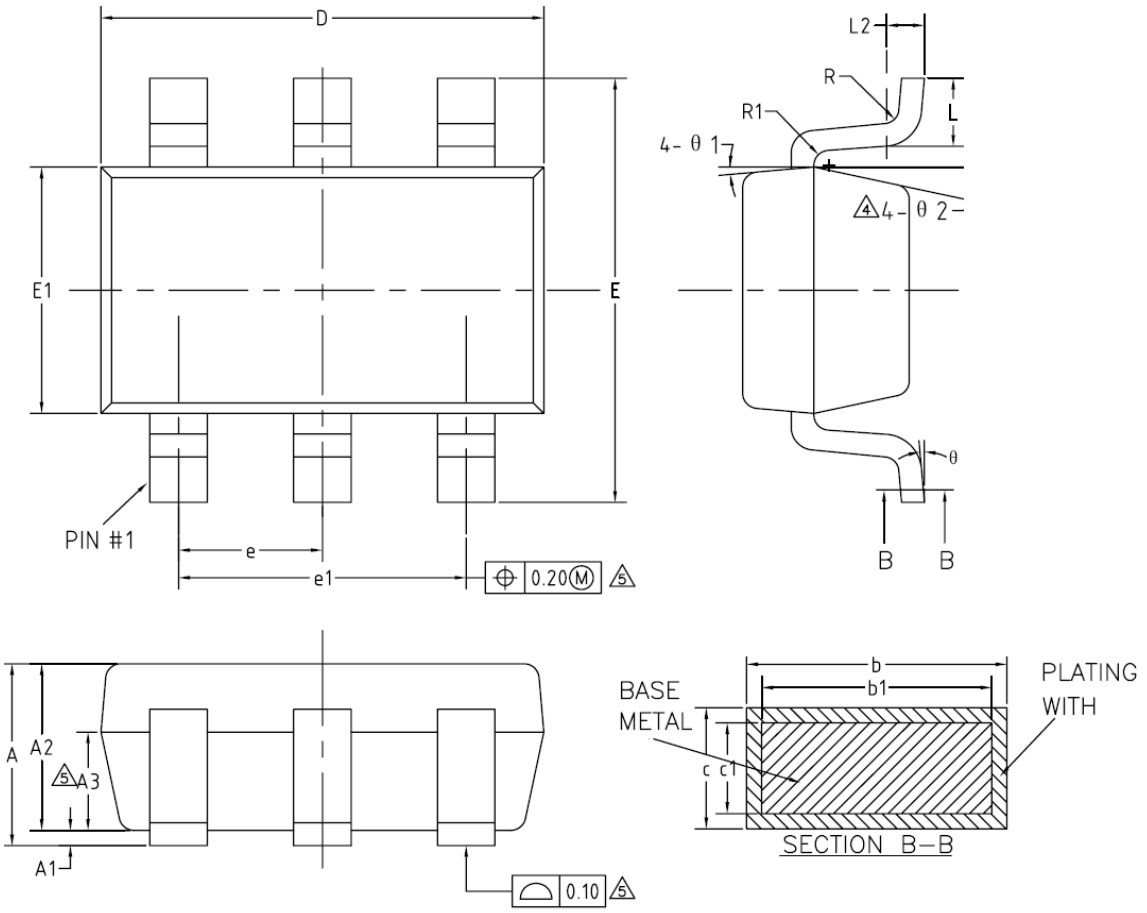


Figure6 SOT23-6 Outline Drawing

Table4 SOT23-6 Package Dimensions

Unit: mm

Symbol	Min	Typ	Max		Symbol	Min	Typ	Max
A	-	-	1.25		e	0.90	0.95	1.00
A1	0	-	0.15		e1	1.80	1.90	2.00
A2	1.00	1.10	1.20		L	0.35	0.45	0.60
A3	0.60	0.65	0.70		L1	0.59RET		
B	0.36	-	0.50		L2	0.25BSC		
b1	0.36	0.38	0.45		R	0.10	-	-
C	0.14	-	0.20		R1	0.10	-	0.20
c1	0.14	0.15	0.16		θ	0	-	8°
D	2.826	2.926	3.026		θ1	3°	5°	7°
E	2.60	2.80	3.00		θ2	6°	-	14°
E1	1.526	1.626	1.726					

8.2 DFN6L(2x2x0.55) Package Dimensions

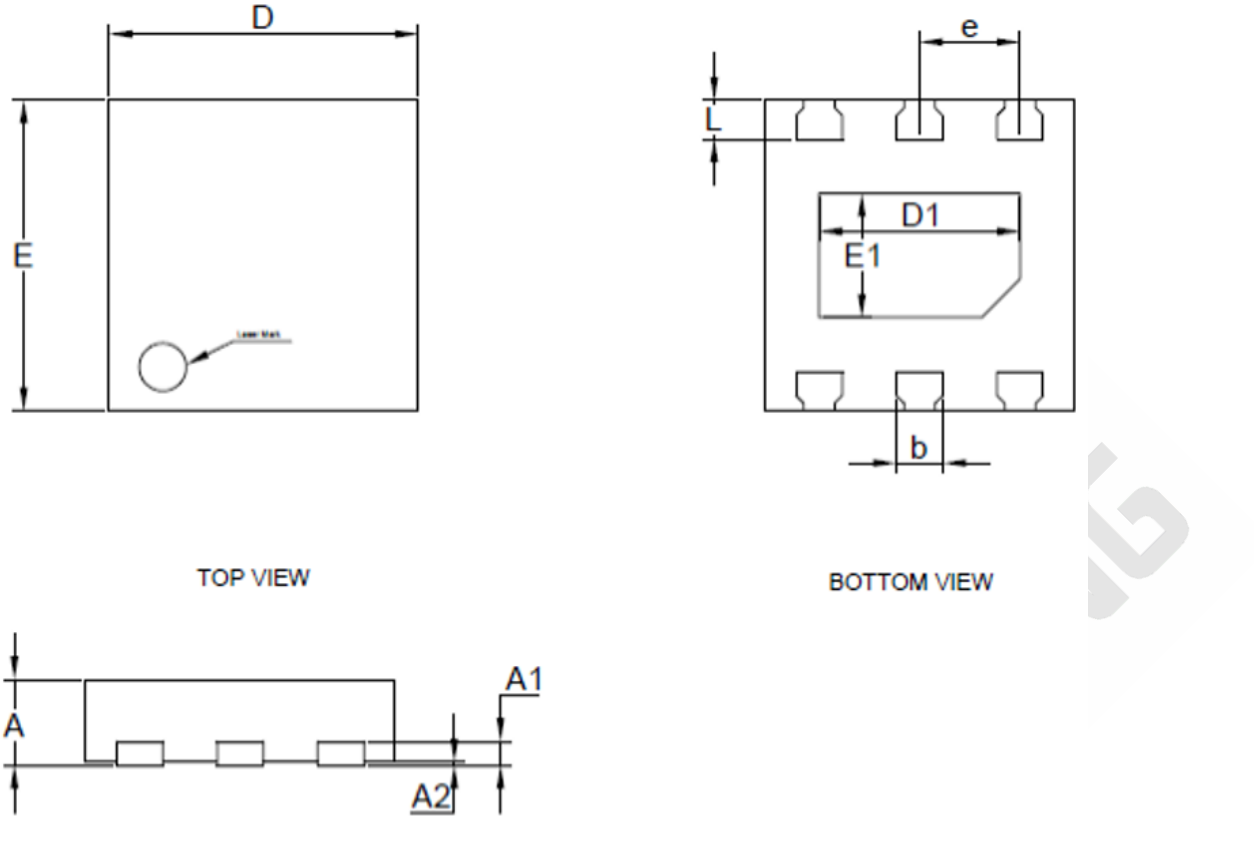


Figure7 DFN2x2-6L Outline Drawing

Table5 DFN2x2-6L Package Dimensions

Unit: mm

Symbol	Min	Typ	Max		Symbol	Min	Typ	Max
A	0.50	0.55	0.60		E1	0.75	0.80	0.85
A1	0.152REF				L	0.20	0.25	0.30
A2	-	0.02	0.05		b	0.25	0.3	0.35
e	0.65BSC							
D	1.95	2.00	2.05					
D1	1.25	1.30	1.35					
E	1.95	2.00	2.05					

8.3 DFN2x2-6L Tape & Reel Specification

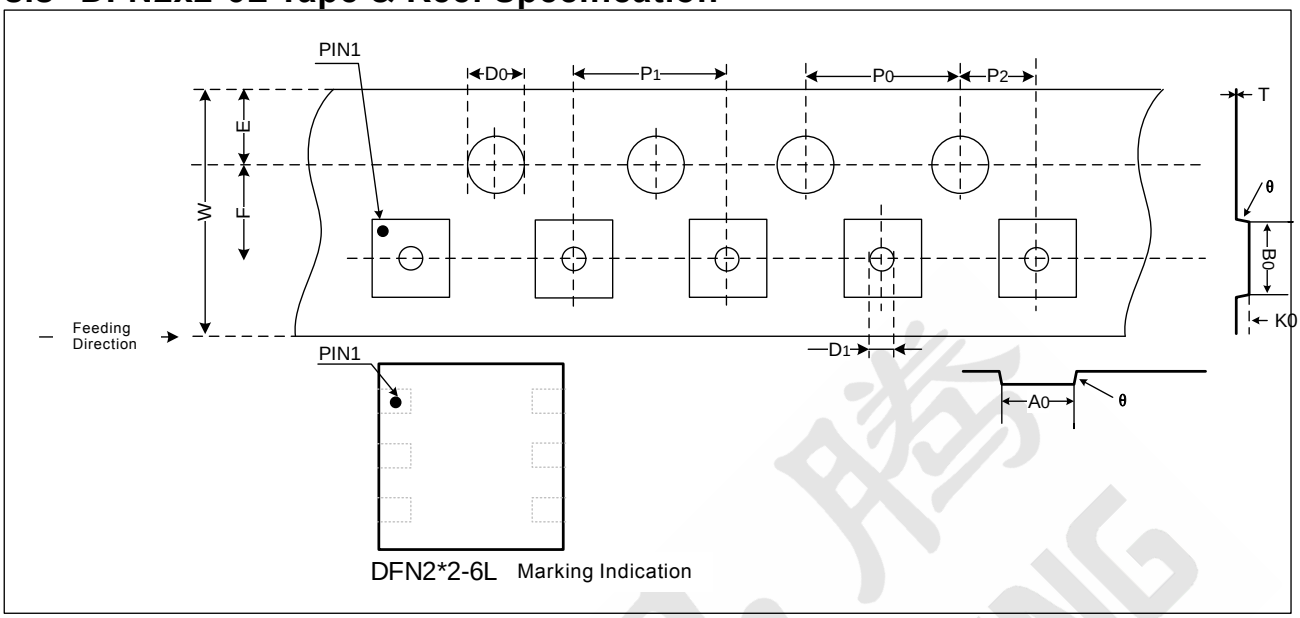


Figure8 DFN2x2-6L Carrier Tape Drawing

Table6 DFN2x2-6L Tape Dimensions

Unit: mm

Symbol	Min	Typ	Max		Symbol	Min	Typ	Max
W	7.9	8.00	8.10		D1	-	1.00	1.10
A0	2.15	2.25	2.35		D0	-	1.50	1.60
B0	2.15	2.25	2.35		P0	3.90	4.00	4.10
K0	0.85	0.95	1.05		P1	3.90	4.00	4.10
E	1.65	1.75	1.85		P2	1.90	2.00	2.10
F	3.40	3.50	3.60		T	0.20	0.22	0.24
					θ		10°	

8.4 DFN4L(1x1x0.45) Package Dimensions

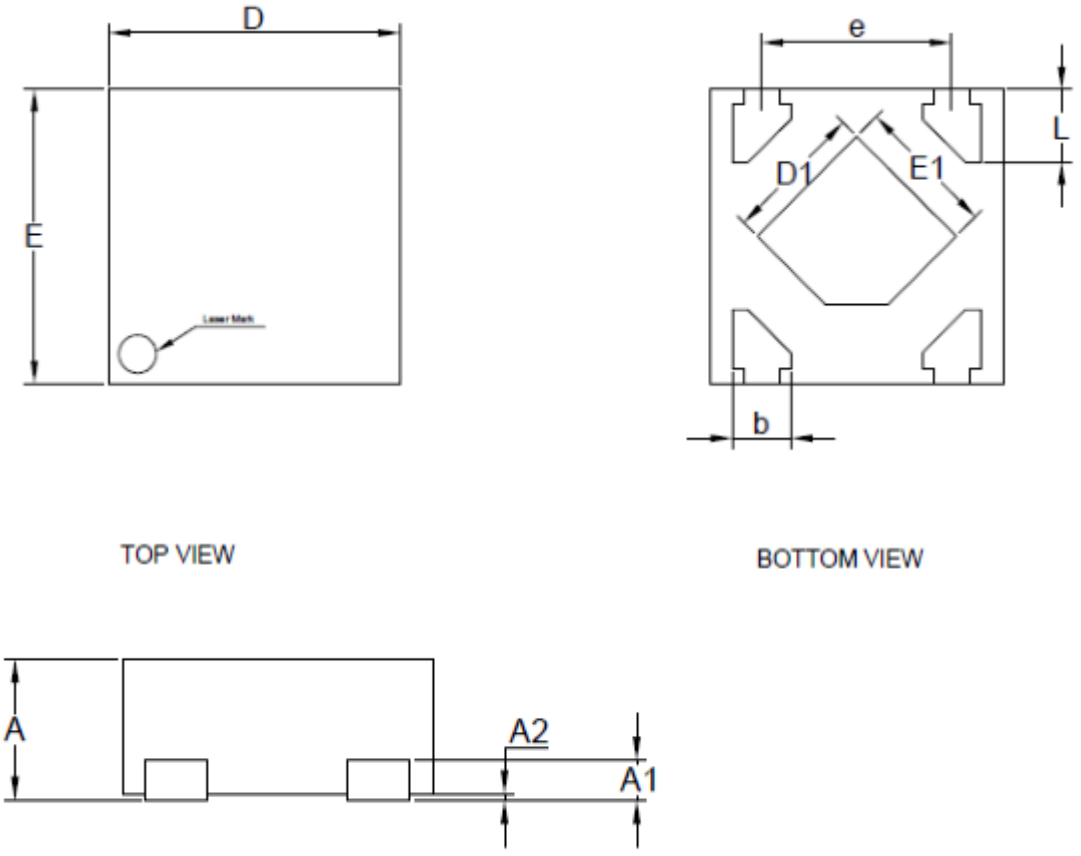


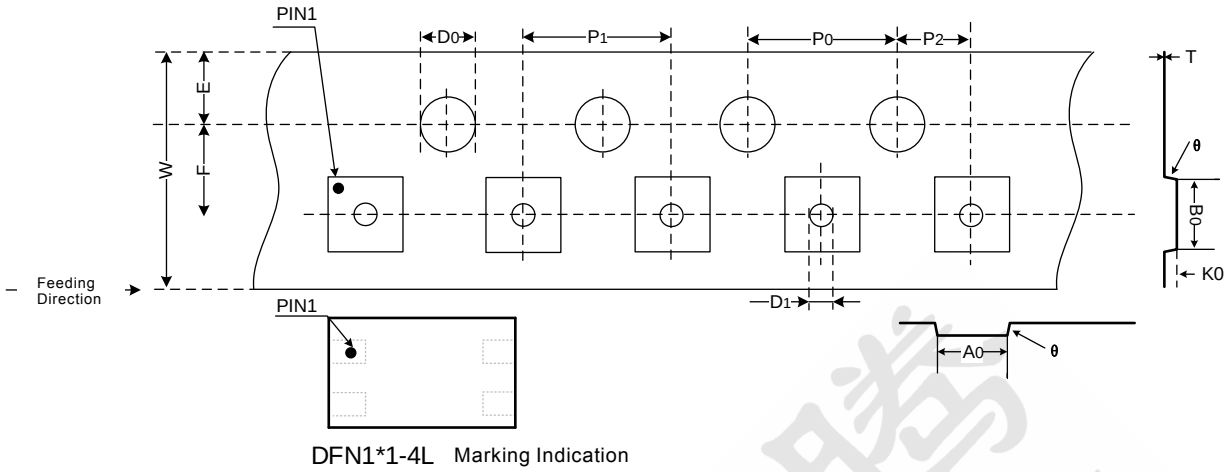
Figure9 DFN1x1-4L Outline Drawing

Table7 DFN1x1-4L Package Dimensions

Unit: mm

Symbol	Min	Typ	Max		Symbol	Min	Typ	Max
A	0.40	0.45	0.50		E	0.95	1.00	1.05
A1	0.127REF				E1	0.43	0.48	0.53
A2	-	0.02	0.05		L	0.20	0.25	0.30
e	0.650BSC							
D	0.95	1.00	1.05					
D1	0.43	0.48	0.53					
b	0.15	0.20	0.25					

8.5 DFN1x1-4L Tape & Reel Specification



DFN1*1-4L Marking Indication

Figure10 DFN1x1-4L Carrier Tape Drawing

Table8 DFN1x1-4L Tape Dimensions

Unit: mm

Symbol	Min	Typ	Max		Symbol	Min	Typ	Max
W	7.9	8.00	8.10		D1	-	0.7	0.8
A0	1.15	1.25	1.35		D0	-	1.50	1.60
B0	1.15	1.25	1.35		P0	3.90	4.00	4.10
K0	0.47	0.57	0.67		P1	3.90	4.00	4.10
E	1.65	1.75	1.85		P2	1.90	2.00	2.10
F	3.40	3.50	3.60		T	0.18	0.23	0.28
					θ		6°	

9. Revision History

Version	Description	Release Date
V1.0	Initial datasheet release	2026-04-13
V1.1	Updated output sink current parameter	2026-04-30
V1.2	Add DFN4 package	2026-06-26

The latest official version shall prevail; download latest document from official website regularly.